REMARKS

This response is being filed in reply to the office action dated February 1, 2005. For the following reasons, this application should be considered in condition for allowance and the case passed to issue.

The indication of allowability of claims 4-6, 9-10, and 13-17 is gratefully acknowledged. However, in light of the arguments presented below, it is believed that the rejected Claims are patentable over the applied references. Accordingly, the Claims indicated as allowable have not been rewritten into independent form at this time.

Claims 1-3, 7-8, and 11-12 were rejected under 35 U.S.C. §102(e) as being anticipated by Lee. These rejections are hereby traversed and reconsideration and withdrawal thereof are respectfully requested. The following is a comparison of the present invention as currently claimed with the Lee reference.

The present invention, as currently claimed in Claim 1, for example, relates to a method of modulating the flatband voltage of the high-k dielectric material of a semiconductor device. This method comprises the step of depositing the high-k dielectric material on the surface. The flatband voltage of the high k dielectric material is controllably modulated by annealing the high-k dielectric material under controlled annealing parameters.

In order to anticipate claims under 35 U.S.C. §102, a single prior art reference must identically disclose each and every element of the claimed invention. For the reasons set forth below, Lee fails to meet this high burden and therefore does not anticipate the claims of the invention.

Lee, U.S. Patent Number 6,844,604, describes a dielectric layer for a semiconductor device and a method of manufacturing this dielectric layer. The high-k dielectric layer, as described in Lee, has one or more ordered pairs of first and second layers. The high-k dielectric layer 14 comprises a metal oxide layer that may be formed using an ALD technique, a MOCVD technique or a reactive sputtering technique. A multi-layer structure is depicted in figures 1B, 1C and 2 of Lee. The high-k dielectric layer 14 is described as being formed by the alternate stacking of two kinds of material layers, such as HfO_2 or ZrO_2 layers and an Al_2O_3 layer. As

described at page 5, line 65, column 6, line 4, the Al_2O_3 layer has much negative fixed charges as compared to the SiO_2 layer, as shown in Figure 3 indicating low frequency C-V plots to the MOS structure having only an Al_2O_3 layer as a high-k dielectric. That is to say, the flatband voltage of the Al_2O_3 layer is shifted towards the direction of positive gate voltage. In this description, it is apparent that the shifting of the flatband voltage of the Al_2O_3 layer in Lee is accomplished by the alternate stacking of layers of different material. Controllable modulation of the flatband voltage is not shown as being achieved by annealing the high-k dielectric material under controlled annealing parameters. There is no description in Lee that shows or suggests the modulation of the flatband voltage as a function of the annealing process or annealing parameters.

Since Lee does not identically disclose the controllable modulation of the flatband voltage of high-k dielectric material by annealing under controlled annealing parameters, Lee cannot be said to anticipate Claim 1 or Claim 11 under 35 U.S.C. §102. Accordingly, the rejection of Claims 1 and 11 under 35 U.S.C. §102 as well as Claims 2-3, 7-8, and 12 which further depend from and define Claims 1 and 11, should be reconsidered and withdrawn. Such action is courteously solicited.

In light of the remarks above, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding this response or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

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To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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